Generalised simulation and experimental implementation of space vector PWM technique of a three-phase voltage source inverter

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Abstract

Adjustable speed drive system requires variable voltage and frequency supply which is invariably obtained from a three-phase voltage source inverter (VSI). A number of Pulse Width Modulation (PWM) schemes are used to obtain variable voltage and frequency supply from an inverter. The most widely used PWM schemes for a three-phase VSI are carrier-based sinusoidal PWM and space vector PWM (SVPWM). There is an increasing trend of using space vector PWM (SVPWM) because of their easier digital realisation and better dc bus utilisation. However, a proper simulation model is still not available in the literature. Thus, this paper focuses on step by step development of MATLAB/SIMULINK model of SVPWM followed by its experimental implementation. Firstly model of a three-phase VSI is discussed based on space vector representation. Next a simple and flexible simulation model of SVPWM is developed using MATLAB/SIMULINK. The developed model is general in nature as it can be utilised to implement both continuous and discontinuous SVPWM. The novelty of the paper relies on the proposal of the flexible and general Matlab/Simulink model of SVPWM. Experimental and simulation results are provided to validate the proposed model.

Keywords: Space vector, PWM, voltage source inverter, discontinuous PWM

1. Introduction

Three-phase voltage source inverters are widely used in variable speed ac motor drives applications since they provide variable voltage and variable frequency output through pulse width modulation control. Continuous improvement in terms of cost and high switching frequency of power semiconductor devices and development of machine control algorithm leads to growing interest in more precise PWM techniques. Volume of work has been carried out in this direction and a review of popular techniques are presented in by Holtz (1992) and Holtz (1994). The most widely used PWM method is the carrier-based sine-triangle PWM method due to simple implementation in both analog and digital realization. However, the dc bus utilization in this method is low \(0.5V_{dc}\). This has led to the investigation into other techniques with an objective of improvement in the dc bus utilization. It is found by Houdsworth and Grant (1984) that injection of zero sequence (third harmonic) extends the range of operation of modulator by 15.5%. The major problem associated with high power drive applications is high switching losses in inverters. To reduce switching losses a PWM technique termed as discontinuous PWM (DPWM) was developed by Depenbrock (1977) and Kolar et al. (1991). The proposed discontinuous PWM techniques were based on triangle-intersection-implementation, in which non sinusoidal modulating signal is compared with triangular carrier wave. A generalized discontinuous PWM algorithm was presented by Hava et al. (1998) which encompasses the techniques presented by Depenbrock (1977) and Kolar et al. (1991). However, the better visualization of the DPWM methods is obtained by using space vector theory. A generalized DPWM based on space vector theory is available in Grahame and Lipo (2000), Kazmierkowski et al. (2002), Dong (2005) and Hava (1998). The discontinuous PWM strategies is based on the principle of eliminating one of the zero voltage vectors, causing the active voltage...
space vectors to join together in two successive half switching interval. The discontinuous PWM techniques have the advantage of eliminating one switching transition in each half switching period, consequently reducing the number of switching by one third. Alternatively, the switching frequency can be increased by 3/2 for the same inverter losses. Another PWM technique termed as Space vector PWM based on space vector theory was proposed by de Broeck et al. (1988) and Ogasawara et al. (1989) which offers superior performance compared to the carrier-based sine-triangle PWM technique in terms of higher dc bus utilization and better harmonic performance. Further this technique offers easier digital realisation. A comprehensive relationship between the carrier-based and SVPWM is illustrated by Holmes (1996) and it was realized that the placement of the active and zero space vectors in each half switching period is the only difference between the carrier-based scheme and SVPWM.

With the advancement in the power semiconductor devices the switching frequency has increased many folds. For high switching frequency applications, Artificial Neural Network (ANN) based space vector PWM technique is developed in Iqbal et al. (2006), Pinto et al. (2000), Kerkman et al. (1991), Haykin (2004), and Muthuramalingam and Himavathi (2007). The implementation of ANN based SVPWM is fast and offers higher bandwidth of control loop and reduced harmonics. The back propagation feed forward network is implemented for gate signal generation required for SVPWM.

This paper is devoted to the development of generalised simulation and experimental approach to implement space vector PWM strategies in continuous and discontinuous modes for three-phase VSIs. The presented simulation method is simple and flexible to incorporate different variant of SVPWM. A similar simulation model is presented by Iqbal et al. (2006), for realising continuous space vector PWM in linear region. However, no experimental results were presented to validate the simulation approach in contrast to this paper where both continuous and discontinuous SVPWM is presented in addition to their experimental verification. Thus, the major contribution of this paper is to present a generalised simple simulation model of the existing technique of SVPWM. At first space vector PWM in linear region is analyzed and a review of the existing DPWM techniques based on space vector approach is presented. The simulation model is developed using the most commonly used MATLAB/SIMULINK environment. The reason for choice of MATLAB/SIMULINK as a development tool is because it is the most important and widely used simulation software and is an integral part of taught programmes in most of the universities in electrical/electronics/computer engineering courses. Codes have been developed but simulation and experimental results are provided for economy of space. The experimental and simulation results match very closely.

2. A review of three-phase VSI modelling

The power circuit topology of a three-phase VSI is shown in Figure 1. Each switch (1, 2,3,4,5 & 6) in the inverter branch is composed of semiconductor devices connected with antiparallel diode. The semiconductor device is a controllable device and diode is for protection.

![Figure 1. Power circuit of a three-phase VSI](image)

Space vector representation of the three-phase inverter output voltages is introduced next. Space vector is defined as:

$$\tilde{v}_i = \frac{2}{3}(v_a \bar{a} + v_b + a^2 v_c)$$

(1)

Where $a = \exp(j2\pi/3)$ and $a^2 = \exp(j4\pi/3)$.

The space vector is a simultaneous representation of all the three-phase quantities. It is a complex variable and is function of time in contrast to the phasor. Phase-to-neutral voltages of a star-connected load are most easily found by defining a voltage difference between the star point $n$ of the load and the negative rail of the dc bus $N$. The following correlation then holds true:
Indices with capital letters are inverter branch voltages and indices with small letters are phase to neutral voltages. $v_{an}$ are called common-mode voltage or zero sequence voltages.

Since the phase voltages in a star connected load sum to zero, summation of equation yields

$$v_{nN} = \frac{1}{3}(v_A + v_B + v_C)$$

Substitution of $v_A$, $v_B$ & $v_C$ yields phase-to-neutral voltages of the load in the following form:

$$v_a = \frac{2}{3}v_A - \frac{1}{3}(v_B + v_C)$$
$$v_b = \frac{2}{3}v_B - \frac{1}{3}(v_A + v_C)$$
$$v_c = \frac{2}{3}v_C - \frac{1}{3}(v_B + v_A)$$

The discrete phase voltage space vector positions thus obtained are shown in Figure 2.

![Figure 2. Phase-to-neutral voltage space vectors](image)

The binary numbers on the Figure 2 indicate the switch state of inverter branch. Here, 1 implies upper switch being on and 0 refers to the lower switch of the branch being on. The most significant bit is for branch A, the least significant bit is related to branch C and the middle is for branch B.

### 3. Continuous space vector PWM

In mid 1980s Space vector pulse width modulation was proposed in Ogasawara et al. (1989) and Holmes (1996), which offer significant advantages over the existing natural and regular sampled sinusoidal PWM. The major advantages include its high performance in terms of better harmonic spectra, ease of implementation and enhanced dc bus utilisation. This section briefly discusses the space vector PWM principle. It is seen in the previous section that a three-phase VSI generates eight switching states which include six active and two zero states. These vectors form a hexagon (Figure 2) which can be seen as consisting of six sectors spanning 60° each. The reference vector which represents three-phase sinusoidal voltage is synthesised using SVPWM by switching between two nearest active vectors and zero vector.

The time of application of active space voltage vectors (as in sector 1 of Figure 2) is found as
\[ t_a = \frac{v_i^*}{v_a} \frac{\sin(\pi/3 - \alpha)}{\sin(2\pi/3)} \]

\[ t_b = \frac{v_i^*}{v_b} \frac{\sin(\alpha)}{\sin(2\pi/3)} \]

\[ t_0 = t_s - t_a - t_b \]  \hspace{1cm} (2)

where \[ \left| v_i^* \right| = (2/3)V_{dc} \]. \( v_i^* \) is the reference vector magnitude, \( \alpha \) is the angle or position of reference vector, and \( t_a, t_b \) & \( t_0 \) are time of applications of vector \( v_a \), vector \( v_b \) and zero vectors, respectively. In order to obtain fixed switching frequency and optimum harmonic performance from SVPWM, each branch should change its state only once in one switching period. This is achieved by applying zero state vector followed by two adjacent active state vectors in half switching period. The next half of the switching period is the mirror image of the first half. The total switching period is thus divided into 7 parts, the zero vector is applied for \( 1/4 \) of the total zero vector time first followed by the application of active vectors for half of their application times and then again zero vector is applied for \( 1/4 \) of the zero vector time. This is then repeated in the next half of the switching period. This is how symmetrical SVPWM is obtained. The branch voltages in one switching period are depicted in Figure 3 for sector I.

The sinusoidal reference space vector form a circular trajectory inside the hexagon. The largest output voltage magnitude that can be achieved using SVPWM is the radius of the largest circle that can be inscribed within the hexagon. This circle is tangential to the mid points of the lines joining the ends of the active space vector. Thus the maximum obtainable fundamental output voltage is

\[ \left| v_i^* \right| = \frac{2}{3} V_{dc} \cos(\pi/6) = \frac{1}{\sqrt{3}} V_{dc} \]  \hspace{1cm} (4)

4. Discontinuous space vector PWM

The distinct feature of space vector PWM is the freedom of explicit pulse placement in half of the carrier cycle. By using this degree of freedom alternative space vector PWM strategy can be formulated in which the active vectors in two successive half switching period are moved to join together, and zero space vector consequently vanishes resulting in Discontinuous Space vector PWM (Houldsworth and Grant, 1984). Due to this manipulation one branch of the inverter remain unmodulated during one switching interval. Switching takes place in two branches and one branch is either tied to the positive dc bus or negative dc bus. The number of switching is thus reduced to 2/3 compared to the continuous SVPWM, hence, the switching losses are reduced significantly. Six different schemes are available depending on the variation in the placement of the zero space vectors.

1. \( T_0 = 0 \) (DPWMMAX)
2. \( T_7 = 0 \) (DPWMMIN)
3. \( 0^\circ \) Discontinuous modulation (DPWM 0)
4. \( 30^\circ \) Discontinuous modulation (DPWM 1)
5. \( 60^\circ \) Discontinuous modulation (DPWM 2)
6. \( 90^\circ \) Discontinuous modulation (DPWM 3)
5. Generalised Matlab/Simulink model of SVPWM

This section details the step-by-step development of a Matlab/Simulink (Pinto et al., 2000) based simulation model for implementing both continuous and discontinuous SVPWM. By slight modification in the Matlab function code different types of SVPWM can be realised. Thus the presented simulation model is general in nature and can be configured very easily to simulate continuous and discontinuous SVPWM in linear modulation range. The simulation model is shown in Figure 4. Each block is further elaborated in Figure 5. Each sub-blocks of Figure 4 is described in the following sub-section.

5.1 Reference voltage generation block

This block is used to simulate balanced three-phase input reference. Three-phase input sinusoidal voltage is generated using ‘function’ block from ‘Functions & Tables’ sub-library of Simulink. This is then converted into two-phase equivalent using Clark’s transformation equations (Holtz, 1992). This is once again implemented using the ‘function’ blocks. Further the two-phase equivalent is transformed to polar form using ‘Cartesian to polar’ block from ‘Simulink extras’ sub-library. The output of this block is the magnitude of the reference as the first output and the corresponding angle of the reference as the second output. The waveform of magnitude is simply a constant line as its value remains fixed. The waveform of angle is shown in Figure 6. It is a saw tooth signal with peak value of ±\( \pi \). Sector identification is done using the comparison of the angle waveform with the predefined values as shown in Figure 6. The number inside the waveform represents the sector number.

5.2 Switching time calculation

The switching time and corresponding switch state for each power switch is calculated in Matlab function block. The Matlab code requires magnitude of the reference, the angle of the reference and timer signal for comparison. The angle of the reference voltage is kept constant for one sampling period using ‘zero order hold’ block so that its value does not change during time calculation. Further, a ramp time signal is required to be generated to be used in Matlab code. The height and width of the ramp signal is equal to the switching time of inverter branch. This ramp is generated using ‘repeating sequence’ from the source sub-library.

The Matlab code should firstly identify the sector of the reference voltage. The time of application of active and zero vectors are then need to be calculated. The times are required to be arranged according to the predefined switching pattern (Figure 3). This time needs to be compared with the ramp timer signal. The height and width of the ramp is equal to the switching period of the inverter branch. Depending upon the location of the time signal within the switching period, the switch state is defined. This switch state is then passed on to the inverter block for further calculation.

5.3 Three-phase inverter block

This block is built to simulate a voltage source inverter assuming constant dc link voltage. The inputs to the inverter block are the switching signals and the outputs are the PWM phase-to-neutral voltages. The inverter model is built using ‘function’ blocks.

5.4 Filter blocks

To visualise the actual output of the inverter block, filtering of the PWM ripple is required. The PWM voltage signal is filtered here using first order filter. This is implemented using ‘Transfer function’ block from ‘Continuous’ sub-library. The time constant of the first-order filter is chosen as 0.8ms. This value is chosen to ensure the cut-off frequency of the low-pass equal to 1250 Hz. So the designed filter will effectively remove the ripple of higher than 1.25 kHz. The value of the filter time constant can be changed if the desired cut-off frequency is different.

5.5 Voltage acquisition

This block stores the output results. The results are stored in ‘workspace’ taken from the ‘sink’ library of the simulink. The filtered phase voltages are stored here.

Simulation is carried out using the developed model for maximum obtainable reference voltage (0.575V\(_{dc}\), Peak) for both continuous and discontinuous SVPWM and the resulting filtered branch and phase voltages are shown in Figure 7 for continuous SVPWM. Average branch, phase and common mode voltages are illustrated for different types of discontinuous SVPWM are elaborated in Figure 8. The input reference fundamental frequency is kept at 50 Hz and the switching frequency of the inverter is chosen as 10 kHz. The output is seen to be sinusoidal without any ripple except the switching harmonics. By simply changing the input reference magnitude and frequency the output voltage magnitude and frequency can be varied. It is observed from Figure 8 that the phase voltage remains sinusoidal for all the cases, the branch voltages and the common mode voltages vary in different schemes.
Figure 4. Matlab/Simulink Model of SVPWM.

Figure 5. Sub-blocks of Matlab/Simulink model, a. Reference voltage generation, b. VSI, c. Filters.

Figure 6. Sector Identification logic.
The relationship between input voltage magnitude and output voltage magnitude is obtained using simulation and the result is illustrated in Figure 9. Total harmonic distortion is calculated up to 25\textsuperscript{th} harmonic using the expression of equation (5) and the relationship between the input reference and THD is plotted in Figure 10.

\[
THD = \sqrt{\sum_{n=3,5,7,...} \left( \frac{V_{n,RMS}}{V_{I,RMS}} \right)^2}
\]

A linear relationship exists between input reference and actual inverter output up to the maximum achievable output (0.575 \(V_{dc}\)). Saturation is then seen in the output due to pulse droppings. THD is seen to decrease (Figure 10) for increase in the input reference up to maximum achievable and then it increases sharply due to overmodulation.

![Figure 7a. Filtered branch voltages for continuous SVPWM](image1)

![Figure 7b. Filtered phase voltages for continuous SV PWM](image2)

![Figure 8. Average branch, phase and common mode voltage, discontinuous SVPWM: a. DPWMMAX, b. DPWMMIN](image3)
Figure 8 (cont’d). Average branch, phase and common mode voltage, discontinuous SVPWM: c. DPWM 0, d. DPWM 1 e. DPWM 2, f. DPWM 3

Figure 9. Relationship between input reference and output voltage.

Figure 10. Relationship between input reference and THD.
6. Experimental implementation

The developed SVPWM schemes for both continuous and discontinuous modes are implemented in real time using Texas Instrument TMS320F2812 DSP and Vi Microsystem, Chennai, India, intelligent power modules. The DSP board is also supplied by Vi Microsystem with integrated interfacing communication board. The PC is connected to the DSP board through printer parallel port. The DSP board is connected through cable to the Inverter intelligent power modules. Current sensors manufactured from LEM, USA are used for feedback purposes. A generalised C++ code is written in the PC for implementing SVPWM similar to the one used for the simulation purpose. The code is run using Code Composer studio CCS 3.2V, and the .out file thus created is then converted to the ASCII file which is loaded to the DSP for further processing. The complete experimental set up is illustrated in Figure 11.

6.1 SVPWM signal generation using TMS320F2812

It is possible to generate six PWM output signals per Event Manager (EV) with programmable dead-band and output polarity using the PWM circuits associated with the compare unit of TMS320F2812. There are two event managers in the DSP namely EVA and EVB. The event manager module of the DSP has built-in hardware to implement SVPWM with great ease. The functional block diagram for of Event Manager A is shown in Figure 12. The functional block diagram of Event Manager B is identical to EVA except that of the corresponding configuration registers. The complete circuit has symmetric/asymmetric waveform generators similar to the general purpose timer, dead-band control unit and output logic.
The following algorithm is used to generate SVPWM outputs (Haykin, 2004).

1. The polarity of the compare output pins are configured by Action Control Register (ACTRx).
2. Compare Command (COMCONx) register is configured to enable compare action and SVPWM operation mode and set the reload condition for Compare register (CMRx).
3. To start the SVPWM operation, GP timer 1 (or GP timer 3, for EVB) should be put in continuous up/down counting mode.
4. The user software needs to determine the voltage $V_{ref}$ to be generated by the inverter in the two dimensional $d$-$q$ plane (direct axis and quadrature axis plane). The two adjacent vectors $V_x$ and $V_{x+60}$ and the time for which each switch remain on $T_1, T_2, T_0$ are determined.
5. The switching pattern corresponding to $V_x$ is loaded in ACTRx (bit 12-14) and 1 in ACTRx (bit 15), or the switching pattern of $V_{x+60}$ is loaded in ACTRx (bot 12-14) and 0 in ACTRx (bot 15).
6. Then CMPR1 is loaded with $(1/2 T_1)$ and CMPR2 with $(1/2 T_1+1/2 T_2)$.

The space vector PWM hardware in the EV module functions as follows:

1. At the beginning of each period PWM outputs are set to the (new) pattern $V_y$ defined by ACTRx (bit 12-14).
2. The PWM outputs switches to the pattern of $V_{y+60}$ if ACTRx (bit 15) is 1 or to the pattern of $V_y$ if ACTRx (bit 15) is 0 ($V_{0,60}=V_{300}, V_{360,60}=V_{60}$) on the first compare match between CMPR1 and GPtimer1 at $(1/2 T_1)$ during up counting.
3. On the second compare match during up counting between CMPR2 and GP timer1 at $(1/2 T_1+1/2 T_2)$ switches the PWM outputs to the pattern (000) or (111), which differs from the second pattern by one bit.
4. On the first compare match during down counting between CMPR2 and GP timer1 at $(1/2 T_1+1/2 T_2)$, switches the PWM outputs back to the second output pattern.
5. On the second compare match during down counting between CMPR1 and GP timer1 at $(1/2 T_1)$, switches the PWM outputs back to the first pattern.

6.2 Experimental results

The experimental results obtained are shown for continuous and discontinuous SVPWM in Figure 13 and Figure 14, respectively. The switching frequency of the inverter is set to 10 kHz and the fundamental frequency is chosen as 50 Hz and the dc link voltage is set to 100 V. The filtered branch voltages and filtered phase-to-neutral voltages for continuous SVPWM illustrated in Figure 13, matches very closely to that of the simulation results (Figure 7). For discontinuous SVPWM, DPWMMAX and DPWMMIN are realised. The filtered branch voltages for the two cases are illustrated in Figure 14. The simulation and experimental results matches very closely in this case as well. The phase-to-neutral voltages are not shown as they are sinusoidal and are identical to Figure 13b. Filtered branch voltages are Digital to analog converter (DAC) outputs of low signals. Filtered phase voltages are high voltages which will be given to the load.
Figure 13. Experimental results continuous SVPWM: a. Filtered branch voltages, b. Filtered phase-to-neutral voltages.

Figure 14. Filtered branch voltages for discontinuous SVPWM a. DPWMMAX, b. DPWMMIN.

7. Conclusions

A simple generalised Matlab/Simulink model is presented to implement both continuous and discontinuous SVPWM for a three-phase VSI. By modifying the switching look-up table in Matlab function code, the two types of SVPWM (continuous and discontinuous) are realised. Variable voltage and variable frequency output is achieved by varying the magnitude and frequency of the input reference values. Experimental set up and configurations of DSP registers are elaborated. The researchers, students and practising engineers can use this concept to verify their model. Both simulation and experimental results are provided. The experimental results match very closely with the simulation results.

Nomenclature

\[ V_{dc} \] DC Link Voltage
\[ v_a, v_B, v_C \] Branch A, B and C, voltages, respectively
\[ v_nN \] Common-mode Voltage
\[ v_a, v_b, v_c \] Phase-to-neutral voltages of Phase A, B and C, respectively
\[ v_s^* \] Reference space vector
\[ t_a, t_b \] Time of application of active space vectors
\[ t_0 \] Time of application of zero space vector
\[ \alpha \] Position of reference space vector

DPWM Discontinuous space vector Pulse width modulation
CMPR Compare register
GP General purpose
ACTR Action control register
EV Event Manager register
DAC Digital to analogue converter

References

Application Note from Texas Instrument, SPRU065E
Haykin S., 2004. Neural Networks, ND Prentice Hall, New York, USA

www.mathworks.co.uk
www.ti.com

Biographical notes

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