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A control strategy based on UTT and I CosΦ theory of three-phase, four-wire UPQC for power quality improvement

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Abstract

This paper presents a control strategy for a three-phase four-wire Unified Power Quality (UPQC) for an improvement of different power quality (PQ) problems. The UPQC is realized by integration of series and shunt active power filters (APFs) sharing a common dc bus capacitor. The shunt APF is realized using a thee-phase, four leg voltage source inverter (VSI) and the series APF is realized using a three-phase, three legs VSI. A control technique based on unit vector template technique (UTT) is used to get the reference signals for series APF, while ICosΦ theory is used for the control of Shunt APF. The performance of the implemented control algorithm is evaluated in terms of power-factor correction; load balancing, neutral source current mitigation and mitigation of voltage and current harmonics, voltage sag and swell and voltage dips in a three-phase four-wire distribution system for different combination of linear and non-linear loads. In this control scheme, the current/voltage control is applied over the fundamental supply currents/voltages instead of fast changing APFs currents/voltages, thereby reducing the computational delay and the required sensors. MATLAB/Simulink based simulations results are obtained, which support the functionality of the UPQC.

Keywords: Power Quality, UPQC, Harmonics, Load Balancing, Power Factor Correction, voltage harmonic mitigation, current harmonic mitigation, voltage sag, swells, voltage dips.

1. Introduction

The availability of sophisticated and more advanced software and hardware for the control systems, the power quality has become one of the most important issue for power electronics engineers. With great advancement in all areas of engineering, particularly, in signal processing, control systems, and power electronics, the load characteristics have changed completely. These nonlinear loads draw non-linear current and degrade electric power quality. The quality degradation leads to low power-factor, low efficiency, overheating of transformers and so on (Gunther *et al.*, 1995). Moreover, in case of the distribution system, the overall load on the system is hardly found balanced, which cause excessive neutral currents of fundamental and harmonic frequencies in a three-phase four-wire distribution system. Ideally, voltage and current waveforms are in phase, power factor of load equals unity, and the reactive power consumption is zero; this situation enables the most efficient transport of active power, leading of the cheapest distribution system. Relating to power quality issues, the designers of power quality conditioner systems are required to follow the recommendations of some world-wide accepted standards like IEEE-519-1992, IEC 1000-3-2, IEC 1000-3-4 recommended practice and requirements for harmonic control in electric power systems. In the past, the solutions to mitigate these identified power quality problems were through using conventional passive filters. But their limitations such as ,fixed compensation, resonance with the source impedance and the difficulty in tuning time dependence of filter parameters have forced the need of active and hybrid filters(Singh *et al.*, 1995; Akagi *et al.*, 1996; Singh *et al.*, 2005) . Under this circumstance, a new technology with a generic name custom power device (CPD) emerged (Ghosh *et al.*, 2002; Hingorani *et al.*, 1995) which is applicable to distribution systems for enhancing the reliability and quality of the power supply.

The Unified Power Quality Conditioner (UPQC) is one of the key CPD to compensate both current and voltage related problems, simultaneously (Aredes *et al.*, 1998; Fujita *et al.*, 1998; Han *et al.*, 2006). As the UPQC is a combination of series and shunt active filters, two active filters have different functions. The series APF suppresses and isolates voltage-based distortions. The shunt APF cancels current-based distortions. At the same time, it compensates reactive current of the load and improves power factor. There are many control strategies reported in the literature to determine the reference values of the voltage and the current of three-phase four-wire UPQC, the most common are the p-q-r theory (Zhili *et al.*, 2006),modified single-phase p-q theory (Khadkikar *et al.*,2009), synchronous reference frame (SRF) theory (Xun *et al.*,2007), symmetrical component transformation (Ghosh *et al.*, 2004) , and unit template technique (UTT) technique (Singh *et al.*,2010) etc. Apart from this one cycle control (OCC) (Chen *et al.*, 2004) (without reference calculation) is also used for the control of three-phase, four-wire UPQC.

The performance of the above mentioned control schemes was mostly affected under distorted and unbalanced supply voltage, while I CosΦ theory (Bhuvaneswari *et al.*, 2008) has potential of working under distorted as well as unbalance supply voltage. Therefore the proposed work presents an application of I CosΦ theory with an in-direct control for the shunt APF of three-phase four-wire UPQC, extending the scheme for four-wire distribution system with additional advantages of fast computation and less numbers of current sensors. In this control algorithm the current/voltage control is applied over the fundamental supply currents/voltages instead of fast changing APFs currents/voltages, thereby reducing the computational delay. Moreover, the load or the filter neutral current are not sensed, thereby reducing the required sensors. In order to mitigate the, voltage harmonics, voltage sag, swells and voltage dips the UTT theory is used because apart from its simplicity, it gives a flexibility to generate the desired reference signals of required amplitude. The proposed control technique is capable of extracting most of the load current and source voltage distortions successfully. The series APF is controlled to eliminate supply voltage harmonics and voltage regulation against voltage sag, swells and voltage dips while, the shunt APF is controlled to alleviate the supply current from harmonics, negative sequence current, reactive power and load balancing.

Current based power quality problems are realized using a combination of linear unbalanced and non-linear loads, while the harmonics, sag, swell and dips in the source voltage is created by switching rectifier load, R-L load, R-C load and an induction motor load, at the point of common coupling (PCC) respectively. This realization of different PQ problems using SIM POWER SYSTEM (SPS), Matlab/ Simulink is very close to realistic working conditions. The UPQC configuration and the load under consideration are discussed in Section 2, the control algorithm for shunt APF and series APF of UPQC is discussed in Section 3 and 4, respectively. The simulation results are discussed in Section 5 and finally Section 6 concludes the paper.

2. System Description and Design

The system under consideration for three-phase four-wire distribution system is shown in Figure1.The UPQC is connected before the load to make the source and the load voltage free from any distortions and at the same time, the reactive current drawn from source should be compensated in such a way that the currents at source side i_s, would be in phase with utility voltages. Provisions are made to realize voltage harmonics, voltage sag and swell in the source voltage by switching on/off the three-phase rectifier load, R-L load and R-C load respectively. A voltage dip in the load voltage is created by switching on an induction motor on the load side. The UPQC, realized by using two voltage source inverters is shown in Figure2. One acting as a shunt APF (Active Power Filter), while the other as series APF. The shunt APF is realized using a thee-phase, four leg voltage source inverter (VSI) and the series APF is realized using a three-phase, three legs VSI. Both the APFs share a common dc link in between them. The four-leg VSI based shunt active filter is capable of suppressing the harmonics in the source currents, negative sequence of source current, load balancing and power-factor correction. The implemented control algorithm consists mainly of the computation of three-phase reference voltages of load voltages (v^*_{la}, v^*_{lb} and v^*_{lc}), and the reference currents for the source current (i^*_{sa}, i^*_{sb} and i^*_{sc}).

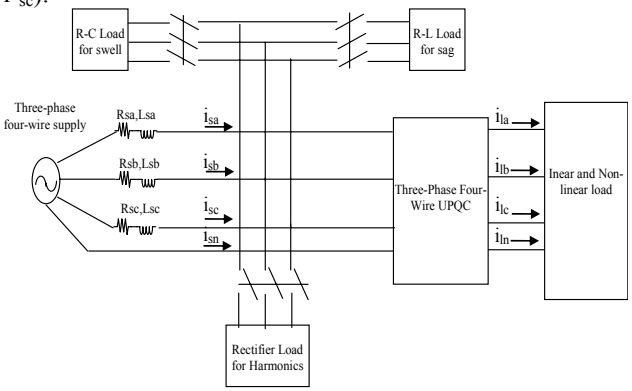

Figure1. System under consideration

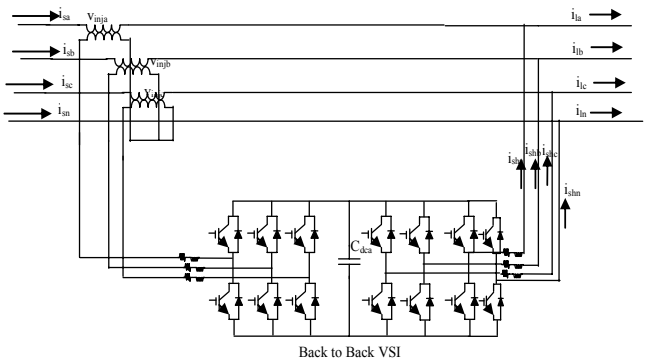

Figure2.UPQC Block Diagram

The voltage at the source side before UPQC, the load voltage at load, the voltage injected by series APF and the dc link voltage between two inverters are represented by v_s, v_L, v_{inj} and V_{dc} respectively. Whereas, the current on the source side, load currents and the current injected by shunt APF are represented by i_s, i_l, and i_{sh} respectively. The source neutral current and load neutral current are represented by i_{sn} and i_{ln}, respectively. The load under consideration is a combination of linear and non-linear loads. Single-phase lagging power-factor load is taken as a linear load, where as a three-phase diode bridge rectifier with a resistive load on dc side is considered as a non-linear load. The values of the circuit parameters and load under consideration are given in Appendix. The selections criteria of interfacing inductor, dc capacitor and ripple filter are given in the following section.

2.1 DC capacitor voltage:

The value of the common link DC bus voltage of back to back connected VSIs of the UPQC depends on the instantaneous energy available to the UPQC (Singh *et al.*, 2004). For a VSI the DC link voltage is defined as

$$V_{dc}=\frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} \tag{1}$$

where m is the modulation index and V_{LL} is the ac line out voltage of UPQC. Considering modulation index as 1 and for line to line voltage (V_{LL} =415 V), the V_{dc} obtained is 677.69 V and is selected as 700 V.

2.2 DC bus capacitor:

The value of dc capacitor (C_{dc}) of back to back connected VSIs of the UPQC depends on the change of DC voltage during increase and decrease of the load. Using the principle of energy conservation, the equation (Singh *et al.*, 2004) for C_{dc} is as follows

$$\frac{1}{2}C_{dc}\left[\left(V_{dc}^2\right)-\left(V_{dc1}^2\right)\right]=3V(\alpha I)t \tag{2}$$

where V_{dc} is the reference dc voltage and V_{dc1} is the minimum voltage level of dc bus, α is the overloading factor, V is the phase voltage, I is the phase current, and t is the time by which the dc bus voltage is to be recovered.

Considering the minimum voltage level of dc the bus, V_{dc1}=690 V, V_{dc}=700 V, V=415/sqrt (3) =239.60 V, I=25.40 A, t=350μs, α=1.2, the calculated value of C_{dc} is 2340μF.Hence C_{dc} is selected as 3000 μF.

2.3ACInductor:

The selection of the ac inductance (L_f) of VSI depends on the current ripple $i_{cr,p-p}$, switching frequency f_s, dc bus voltage (V_{dc}), and L_f is given as (Singh *et al.*, 2004)

$$L_f=\frac{\sqrt{3}mV_{dc}}{12\alpha f_s i_{cr(p-p)}} \tag{3}$$

where m is the modulation index and α is the overload factor. Considering, $i_{cr,p-p}$=2.5%, f_s=10 KHz, m=1,V_{dc}=700 V, α=1.2, the L_f value is calculated to be 4.88 mH. A round-off value of L_f of 5 mH is selected in this work.

2.4Ripple Filter:

A low-pass first-order filter at half the switching frequency is used to filter the high-witching frequency noise from the injected voltage of series APF. Considering a low impedance of 8.1Ω for the harmonic voltage at half the switching frequency 10 KHz /2=5 KHz, the ripple filter capacitor is designed as C_f =5μF. A series resistance (R_f) of 7 Ω is included in series with the capacitor (C_f).The impedance is found to be 638Ω at fundamental frequency, which is sufficiently large, and, hence, the ripple filter draws negligible fundamental current.

3. Control Scheme of Series APF

The series is controlled in such a way that it injects voltages ($v_{inj,}$ v_{injb} and v_{injc}), which cancel outs the distortions present in the supply voltages ($v_{sa,}$ v_{sb} and v_{sc}), thus making the voltages at PCC ($v_{la,}$ v_{lb} and v_{lc}) perfectly sinusoidal with the desired amplitude. In other words, the sum of supply voltage and the injected series filter voltage makes the desired voltage at the load terminals. The control strategy for the series APF is shown in Figure3. Since, the supply voltage is distorted, a phase locked loop (PLL) is used to achieve synchronization with the supply voltage (Singh *et al.*, 2010) .Three-phase distorted supply voltages are sensed and given to PLL which generates two quadrature unit vectors (sin*wt*,coswt).The in-phase sine and cosine outputs from the PLL are used to compute the supply in phase,120^o displaced three unit vectors (u_a ,u_b u_c) using eqn.(4) as:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \tag{4}$$

The computed three in-phase unit vectors then multiplied with the desired peak value of the PCC phase voltage (V^*_{lm}), which becomes the three-phase reference PCC voltages as:

$$\begin{bmatrix} v^*_{la} \\ v^*_{lb} \\ v^*_{lc} \end{bmatrix} = V^*_{lm} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{5}$$

The desired peak value of the PCC voltage under consideration is 338V (=415sqrt (2)/sqrt(3)).The computed voltages from reference voltages from eqn.(5) are then given to the hysteresis controller along with the sensed three phase PCC voltages(v_{la}, v_{lb} and v_{lc}).The output of the hysteresis controller is switching signals to the six switches of the VSI of series APF. The hysteresis controller generates the switching signals such that the voltage at PCC becomes the desired sinusoidal reference voltage. Therefore, the injected voltage across the series transformer through the ripple filter cancels out the harmonics, voltage sag, swells and voltage dips present in the supply voltage.

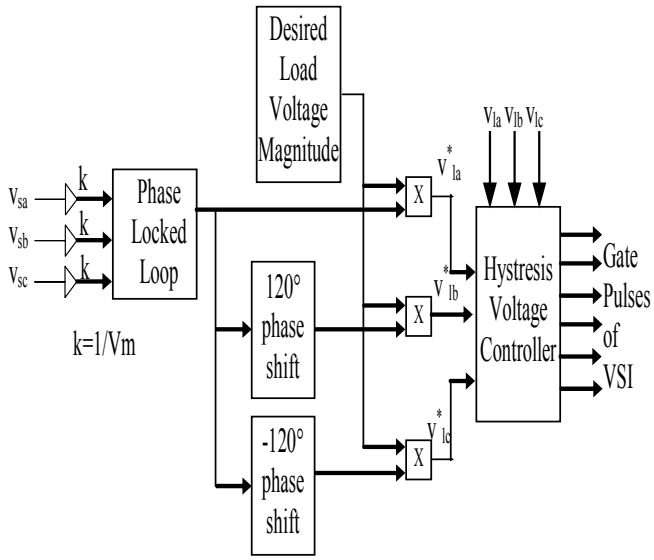

Figure3. Control Scheme of Series APF using UTT

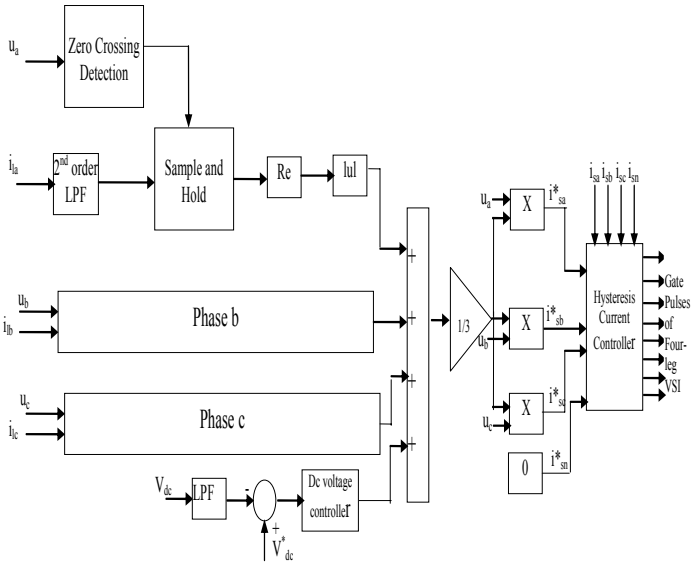

Figure4. Control Scheme of Shunt APF using ICosΦ Theory

4. Control Scheme of Shunt APF

The control algorithms for shunt APF consists of the generation of 3-phase reference supply currents (i^*_{sa}, i^*_{sb} and i^*_{sc}). In this proposed control algorithm, the sensed(i_{sa}, i_{sb} and i_{sc}) and reference source currents(i^*_{sa}, i^*_{sb} and i^*_{sc}) are compared in a hysteresis current controller to generate the switching signals to the switches of the shunt APF which makes the supply currents sinusoidal, balanced in- phase with the voltage at PCC. Hence the supply current contains no harmonics or reactive power component. The control algorithm based on the modified ICosΦ algorithm is shown in Fig.4.

The amplitude of active component of fundamental load currents are given as:

$$\left|\mathrm{Re}(I_{La1})\right| = \left|I_{La}\right| Cos\phi_a ; \left|\mathrm{Re}(I_{Lb1})\right| = \left|I_{Lb}\right| Cos\phi_b ; \left|\mathrm{Re}(I_{Lc1})\right| = \left|I_{Lc}\right| Cos\phi_c \tag{6}$$

The amplitude of active component (ICosΦ) of fundamental load current is extracted at zero crossing of the unit template in phase of PCC voltage from the load currents by +90^o, using a set of low pass filters. The filters are with 50 Hz cut-off frequency to extract the fundamental load current. A Zero crossing detector and a "sample and hold" circuit are used to extract the ICosΦ (amplitude of fundamental load current at zero crossing of corresponding in phase unit template).For balance source currents, the magnitude of active component of reference source currents can be expressed as :

$$I^*_{sP} = \left(\left|I_{La}\right| Cos\phi_a + \left|I_{Lb}\right| Cos\phi_b + \left|I_{Lc}\right| Cos\phi_c + I_d\right) / 3 \tag{7}$$

where $|I_{La}|Cos\,\phi_a; |I_{Lb}|Cos\,\phi_b; |I_{Lc}|Cos\,\phi_c$, are the amplitude of the load active currents and I_d is the output of Dc bus voltage PI controller for self supporting bus of the UPQC which can be expressed as;

$$I^*_{d(n)} = I^*_{d(n-1)} + K_{pd}\{V_{de(n)} - V_{de(n-1)}\} + K_{id}V_{de(n)} \tag{8}$$

where $V_{de(n)} = V_{dcr} - V_{dca(n)}$ denotes the error in V_{dc} calculated over reference value of V_{dc}. and average value of V_{dc}.K_{pd} and K_{id} are proportional and integral gains of the dc bus voltage PI controller. The three-phase component of source currents can be obtained with in-phase unit templates as:

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = I^*_{sp} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{9}$$

In this proposed control algorithm, the sensed(i_{sa}, i_{sb} and i_{sc}) and reference source currents(i^*_{sa}, i^*_{sb} and i^*_{sc}) are compared in a hysteresis current controller to generate the switching signals to the switches of the shunt APF which makes the supply currents sinusoidal, balanced in in- phase with the voltage at PCC. Hence the supply current contains no harmonics or reactive power component. The source neutral current is compensated to fallow a reference signal of zero magnitude by switching the fourth leg of the VSI, through the hysterisis controller. By doing this, the supply neutral current can be eliminated. In this control scheme, the current control is applied over the fundamental supply currents instead of the fast changing APF currents, thereby reducing the computational delay and number of required sensor. In addition to this, the load or the filter neutral current are not sensed, thereby reducing the required sensors.

5. Results and Discussion

The proposed control scheme has been simulated using MATLAB/ Simulink and its Sim-Power System toolbox. The performance of UPQC is evaluated in terms of voltage and current harmonics mitigation, load balancing, power-factor correction and mitigation of voltage sag, swells and voltage dips under different load conditions.

5.1 Performance of UPQC for power-factor correction and load balancing: Figure 5 shows the response of UPQC with linear lagging power-factor load for power-factor correction and load balancing.

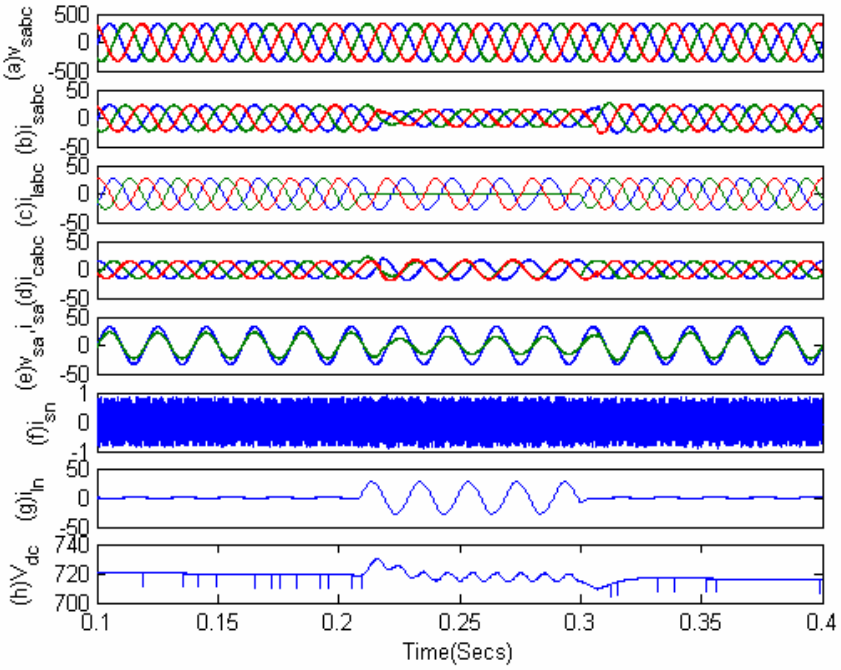

Figure5. Performance of UPQC for load balancing and power factor correction

The shunt APF is put into operation at 0.1 sec. Figure5 (e) shows that after 0.1 sec the source voltage and source current in phase 'a' are exactly in phase. At t=0.2 sec the load is changed from three phase to two phase to make the load unbalanced and restored to three-phase balanced load at t=0.3 sec. Figure 5(b)shows that source current ale balanced and in phase with respective source voltages during unbalanced load operation. During this period, a current 19.24A RMS (i_{ln}) flows in the neutral conductor as shown in Figure5 (g). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Figure5 (f). It is also observed from Figure5 (h) that during unbalanced load operation, the dc voltage is maintained to its reference value.

5.2 Performance of UPQC for power-factor correction, load balancing and current harmonic mitigation: Figure 6 shows the response of UPQC for power-factor correction, load balancing and current harmonic mitigation. In order to demonstrate the response of UPQC for load balancing, power factor correction and current harmonic mitigation, the load under consideration is a combination of a three-phase diode bridge rectifier with resistive load and and two single phase lagging power factor load in phase 'a' and 'b' only. Because of this unbalanced load, a current 16.86A RMS (i_{ln}) flows in the neutral conductor as shown in Figure 6 (g). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Figure 6 (f). It is observed that the supply currents are balanced, sinusoidal and in-phase with the voltages as is shown in Figure 6 (b).

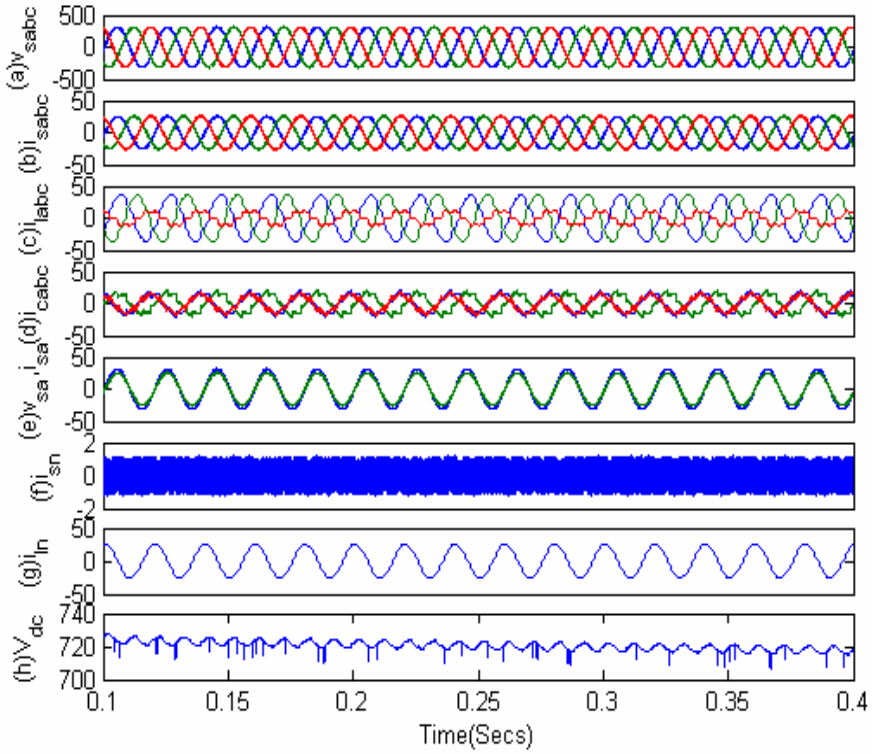

Figure 6. Performance of UPQC for load balancing, power factor correction and current harmonic mitigation

5.3 Performance of UPQC for power-factor correction, load balancing, current and voltage harmonic mitigation: Figure 7 shows the response of UPQC for load balancing, power factor correction, voltage harmonic mitigation and current harmonic mitigation. In order to verify the effectiveness of control algorithm for voltage harmonic mitigation, a three-phase diode bridge rectifier with resistive load on dc side is switched on at 0.05 sec. Because of this the voltage across the load becomes distorted. To visualize the shunt APF and series APF performance individually, both APF's are put into operation at different instant of time. At time t_1=0.1 sec, shunt APF is put into operation first. It is observed from Figure 7 (d) that the supply currents are balanced; sinusoidal and in-phase with the voltages even under non-sinusoidal utility voltage. The source current THD in phase 'c' is improved form 15.28 % to 3.21 %. At time t_2=0.25 sec the series APF is put into the operation. The series APF starts compensating voltage harmonics immediately by injecting out of phase harmonic voltage, making the load voltage at load distortion free. The voltage injected by series APF is shown in Figure 7(c). Here load voltage THD is improved form 6.05 % to 1.11 %. The harmonic spectra of the source current and the load voltage in phase 'c' with compensation and without compensation are shown in Figure 8. Because of

unbalanced load, a current 18.60A RMS (i_{ln}) flows in the neutral conductor as shown in Figure 7 (i). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Figure 7 (h).

5.4 Performance of UPQC for power-factor correction, load balancing, current harmonics and voltage sag mitigation: The simulation results for voltage sag compensation are shown in Figure 9. There are four instants; t_1, t_2, t_3 and t_4. At time t_1=0.10 s, the shunt APF is put into the operation and its operation is as discussed previously. At time t_2=0.25 s, series APF is put into operation. Now a 10 kW, 40 Kvar (inductive) load is switched on at t=0.35 s and switched off at t=.045 sec. Because of this a sag is developed on the system at time t_3=0.35 s. This sag lasted till time t_4=0.45 s, as shown in Figure 9 (a). After time t_4=0.45 s, the system is again at normal working condition. During this voltage sag condition, the series APF is providing the required voltage by injecting in phase compensating voltage equals to the difference between the reference load voltage and supply voltage, as shown in Figure 9 (c). The load voltage profile in Figure 9 (b) shows that UPQC is maintaining it at desired constant voltage level at load even during the sag on the system such that the loads cannot see any voltage variation. Because of unbalanced load, a current (i_{ln}) flows in the neutral conductor as shown in Figure 9 (i). This current is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Figure 9 (h).

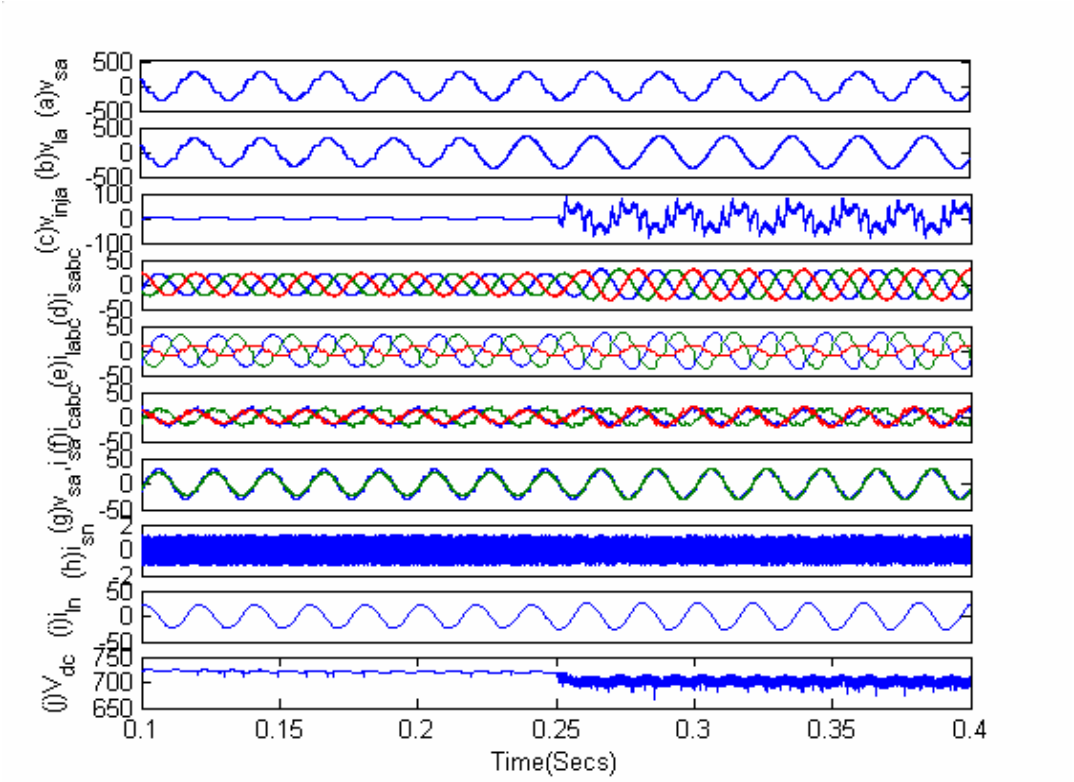

Figure 7. Performance of UPQC for load balancing, power factor correction, current and voltage harmonic mitigation

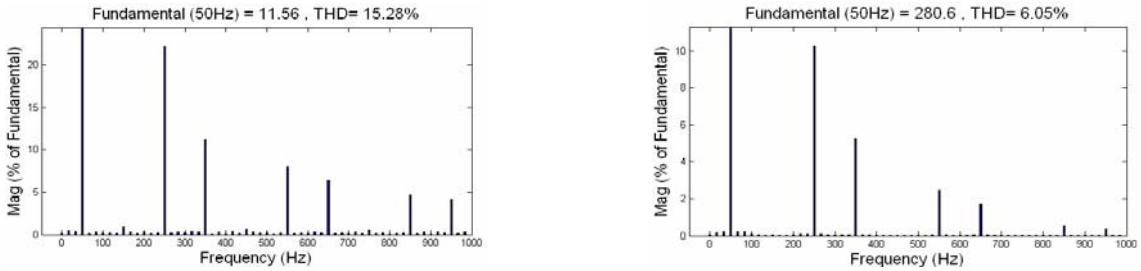

Figure 8. (a) - (b) Source current and Load voltage without compensation

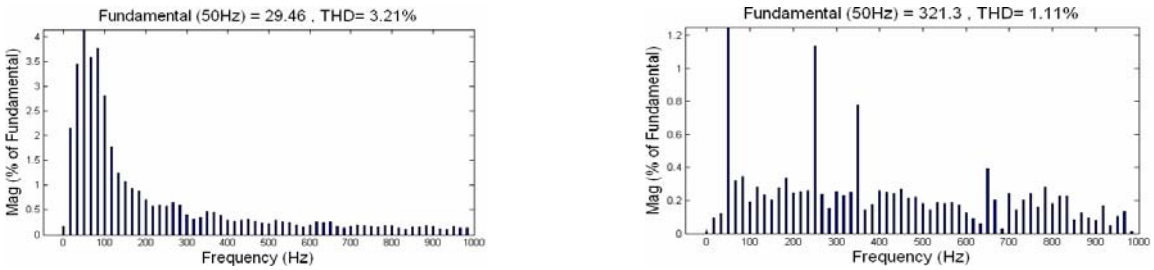

Figure 8.(c) - (d) Source current and Load voltage with compensation

5.5 Performance of UPQC for power-factor correction, load balancing, current harmonics and voltage swell mitigation: At time t_1=0.10 s, the shunt APF is put into the operation and at time t_2=0.20 s, series APF is put into operation. A swell is now introduced on the system by switching on a 10 kW, 40 Kvar (capacitive) from time t_3=0.35 s to t_4=0.45 s, as shown in Figure 10. Under this condition the series APF injects an out of phase compensating voltage in the line through series transformers, equal to the difference between the reference load voltage and supply voltage, as shown in Figure 10 (c). The load voltage profile in Figure 10 (b) shows the UPQC is effectively maintaining the load bus voltage at desired constant level. Figure 10 (i) shows that a current (i_{ln}) flows in the neutral conductor, which is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Figure 10 (h).

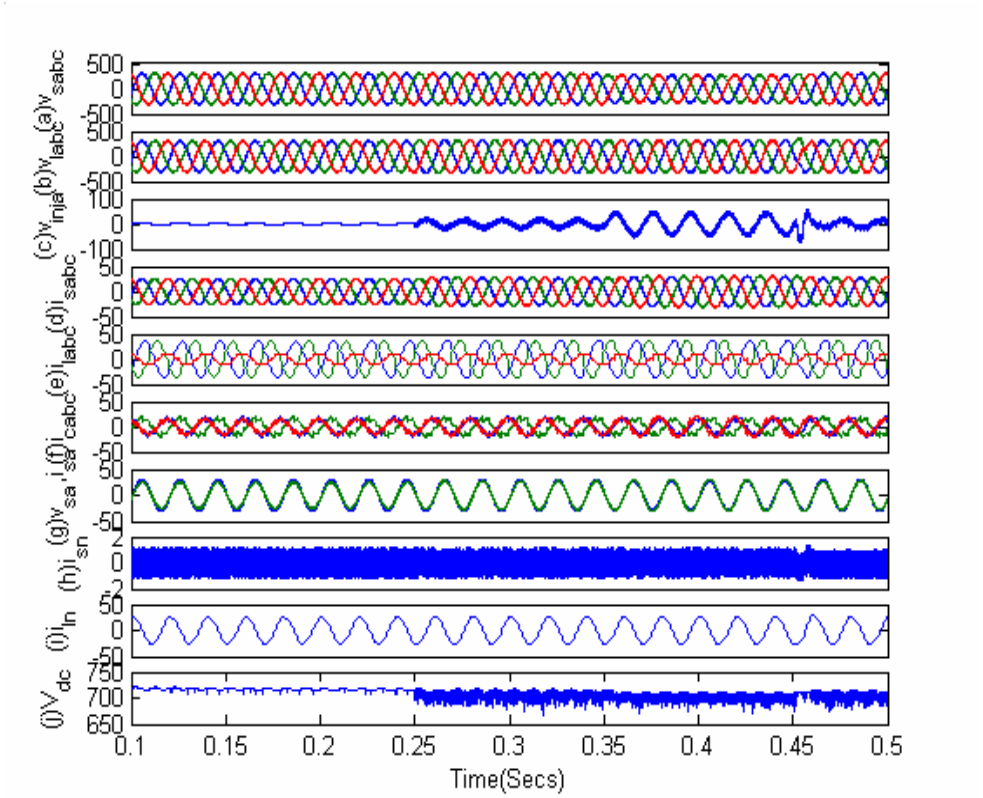

Figure.9 Performance of UPQC for load balancing, power factor correction, current harmonic and voltage sag mitigation

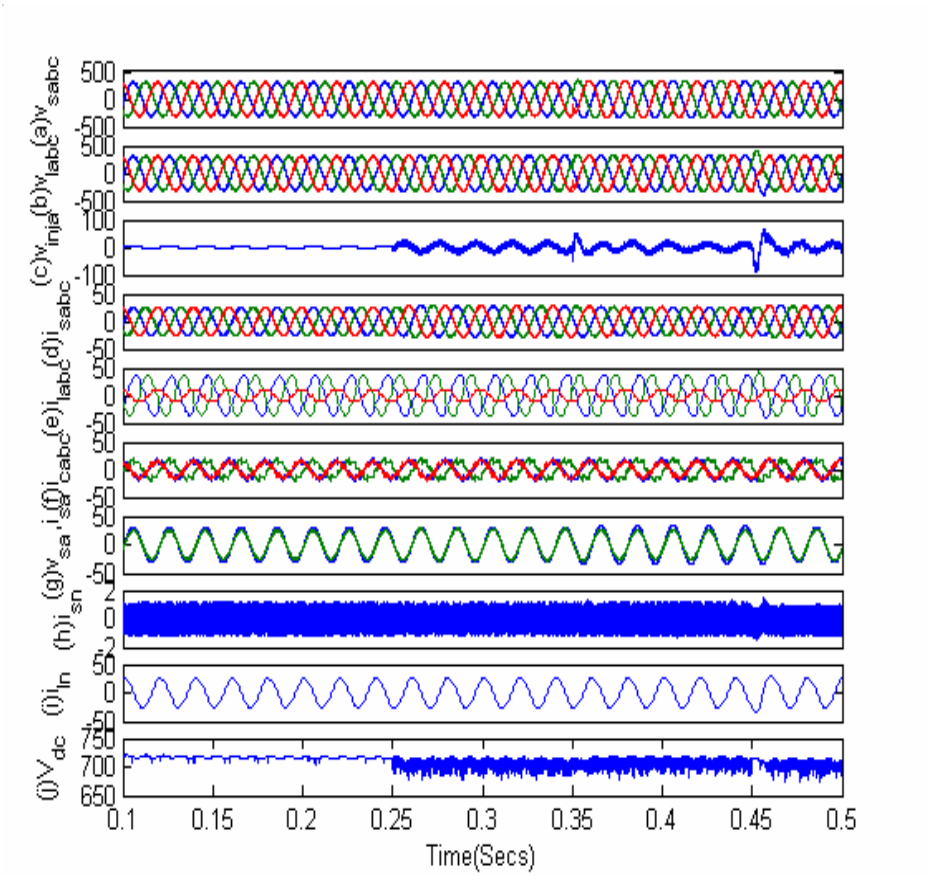

Figure 10. Performance of UPQC for load balancing, power factor correction, current harmonic and voltage swell mitigation

5.6 *Performance of UPQC for power-factor correction and voltage dips mitigation:* Fig 11 shows the response of the UPQC during the stat up of an induction motor. An induction motor load is a typical load on the supply system. An induction motor draws a heavy inrush current, which leads to a voltage dip. Both the shunt and series APF are switched on at 0.05sec. An induction motor load is connected at t=0.15sec.There is high inrush current during the starting of the induction motor as shown in Fig.11 (d). The series APF injects in phase compensating voltage equals to the difference between the reference load voltage and actual load voltage, as shown in Fig. 11 (c). The load voltage profile in Fig.11 (b) shows the UPQC is effectively maintaining the load voltage at desired constant level even during starting of an induction motor and there is no voltage dip. In addition to this, Fig.11 (g) shows that the voltage and current are in phase even during heavy inrush current.

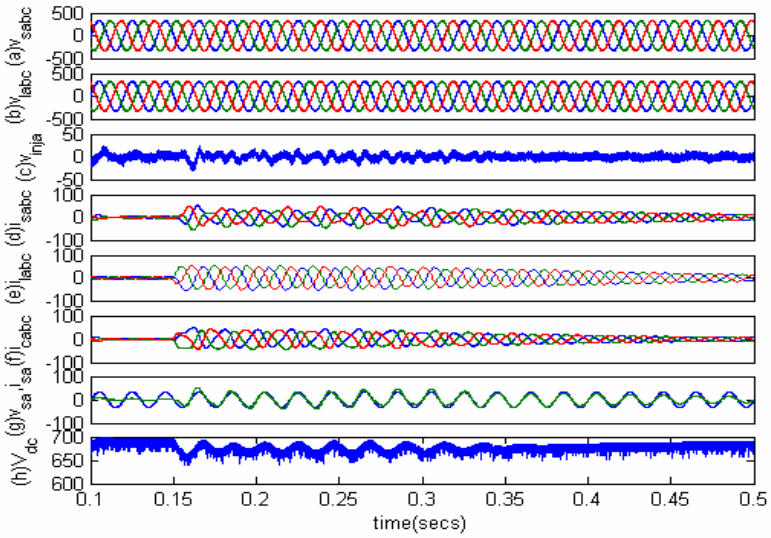

Figure 11. Performance of UPQC for power-factor correction and voltage dip mitigation

5.7 Performance of UPQC during sudden load change: In order to show the response of UPQC for sudden load change the load across the dc side of the rectifier is increased at t=0.25 s. It is observed from Figure 12(b) that in addition to the load balancing, power factor correction and current harmonic mitigation, the UPQC controller acts immediately without any delay in the operation and gain the new steady state. It is also observed from Figure 12 (f) that there is small dip in dc voltage at t=0.25 s, but dc link is able to regulate the dc voltage to its previous value. Figure 12 (i) shows that a current (i_{ln}) flows in the neutral conductor, which is compensated for by the fourth leg of the shunt APF, thus reducing the supply neutral current (i_{sn}) to zero as depicted in Figure 12 (h).

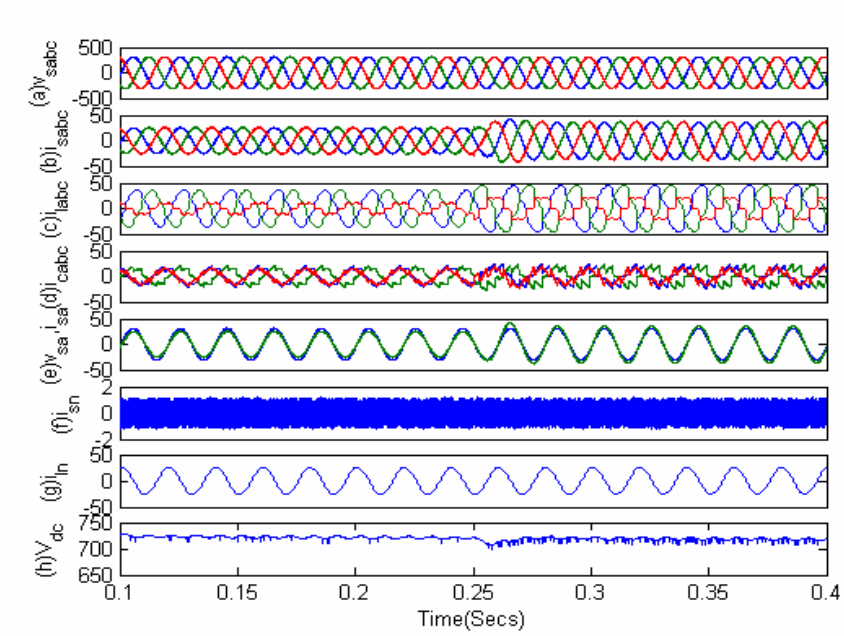

Figure 12. Performance of UPQC during sudden load change

6. Conclusion

A control scheme for power quality improvement in a three-phase four-wire distribution system has been proposed and investigated in a very close to realistic working conditions. In this scheme, the UPQC reference signals generation is carried out using the combination of UTT and I CosΦ theory. The proposed approach has not been reported in literature for three-phase four-wire UPQC. The scheme is an extention of ICosΦ theory for four-wire distribution system, which results in fast computation and reduced number of current sensors. The computational delay and the number of sensors are reduced by indirectly controlling the three-phase supply currents and the source neutral current. The performance of the UPQC has been observed to be satisfactory for various power quality improvements like load balancing; source neutral current mitigation, power-factor correction, voltage and current harmonic mitigation, mitigation of voltage sag and swells. Further the performance of system under consideration was evaluated and found satisfactory under the case of voltage dip, demonstrating the strength of proposed scheme. It is observed that supply currents and load voltage harmonic levels are maintained below IEEE-519 standards. Moreover, the performance of UPQC has been found satisfactory during transient conditions. The rating and the number of VSI switches of UPQC can be further improved by integrating passive elements (i.e star-delta transformer or other transformer configurations) for source neutral current mitigation. The experimental setup and the results are planned for future work.

Appendix

The system parameters used are as follows:
Supply voltage and line impedance: 415 V L-L, f=50 Hz, R_s=0.1ohm, L_s=1.5mH
Filter:R=7ohm,C=5μF
DC bus capacitance: C_{dc}=3000μF
DC bus voltage:700V
Transformer: 250MVA, 58kV/12kV
K_p=K_i=2
Loads: Two single-phase linear load of 12KW, 8KVar in phase ‘a’ and ‘b’ only and a Three-Phase Rectifier Load R=50 ohm on dc side

Induction Motor Load: 3 HP, 50 Hz, 415 V L-L, wound rotor

References

Akagi, H,1996 New trends in active Filters for power conditioning. *IEEE Trans.on Ind. Appl*., pp. 1312–1322.

Aredes, M., K. Heumann, and E. H. Walandble, 1998. An universal active power line conditioner. *IEEE Trans. Power Del.*, Vol. 13, No. 2, pp. 545–551.

Bhuvaneswari, G., Nair, M.G. 2008.Design, Simulation and analog Circuit Implementation of a Three-Phase Shunt Active Filter Using the ICosΦ Algorithm. *IEEE Trans. on Power Delivery*, Vol.23,pp.1222-1235.

Chen, G., Y. Chen and K.M. Smedley,2004.Three-phase four-leg active power quality conditioner without references calculation., *Procd. IEEE APEC '04*, Vol.1, pp.587-593.

Fujita, H. and H. Akagi, 1998. The unified power quality conditioner: the integration of series- and shunt-active filters. *IEEE Trans. Power Electron.*, Vol. 13, No. 2, pp. 315–322.

Gunther, E.W. and H.Mehta, 1995. A survey of distribution system power quality. *IEEE Trans. on Power Delivery*, Vol. 10, No. 1, pp. 322-329.

Ghosh,A. and G. Ledwich,2002. *Power Quality Enhancement Using Custom Power Devices.*Kulwer International Series in Engineering and Computer Science.

Ghosh, A.,A.K. Jindal and A. Joshi,2004. A unified power quality conditioner for voltage regulation of critical load bus. *Proc. IEEE Power Eng. Society General Meeting,* , Vol.1, pp. 471-476**.**

Han, B., B. Bae, H. Kim, and S. Baek, 2006.Combined operation of unified power-quality conditioner with distributed generation. *IEEE Trans. Power Del.*, Vol. 21, No. 1, pp. 330–338.

Hingorani, N. G., 1995. Introducing custom power. *Proc. IEEE Spectrum*, Vol.32, pp. 41-48.

Khadkikar, V. and A. Chandra,2009. A novel structure for three-phase four-wire distribution system utilizing unified power quality conditioner (UPQC).*IEEE Trans. Industry Applications*, Vol.45, pp.1897-1902.

Singh, B., AL.K. Haddad and A. Chandra, 1999. A review of active filters for power quality improvement. *IEEE Trans. on Ind. Electron,* Vol.46, pp. 960–971.

Singh, B., V. Verma, A. Chandra and K. Al-Haddad, 2005. Hybrid filters for power quality improvement.Proc. *IEE on Generation, Transmission and Distribution*, Vol.152, pp.365-378.

Singh, B. and Venkateswarlu, 2010.A Simplified Control Algorithm for Three-Phase Four-Wire Unified Power Quality Conditioner. *Journal of Power Electronics*, Vol.10, No.1.pp-91-96.

Singh B.N., Rastgoufard P., Singh B., Chandra A. and Haddad K.A., 2004. Design, simulation and implementation of the three pole/four pole topologies for active filters. *Inst. Elect. Engg. Proc. Electr. Power Appl.*, Vol.151, pp.467-476.

Xun, Li.,Zhu. Guorong ,Duan. Shanxu and Chen Jian Chen,2007. Control Scheme for Three-Phase Four-Wire UPQC in a Three-Phase Stationary Frame. *Procd.IEEE/IECON 2007*, pp.1732-1736.

Zhili, T.,Li Xun, Chen Jian, Kang Yong and Duan Shanxu, 2006. A direct control strategy for UPQC in three-phase four-wire system. *Proc. IEEE Conf. on Power Electron. and Motion Control 2006*, Vol.2, pp.1-5.

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